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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/470,329	BENNETT ET AL.	
	Examiner	Art Unit	
	Denise Tran	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2008* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/10/08 has been entered.

2. The applicant's amendment filed 3/10/08 has been considered. Claims 1-21 are presented for examination.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed limitations, claim 1, "retrying the first bus transaction and each subsequent non modifying bus transaction for the shared resource until the status bit is clear;" claim 10, "wherein the status indicator is a status bit to indicate whether the second bus transaction completes, if the nonmodifying bus transactions complete, the status bit is cleared, otherwise status bit remains as being set", claim 3, "clearing the status bit randomly;" claim 4, "clearing the status bit at periodic intervals;" claim 5, "wherein the periodical intervals are longer than a length of time for a bus transaction to complete;" claim 6, " clearing the status bit using a pseudo-random method," and claims 7-9, 15, 17 have similar problems as

discussed above, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The objection to the drawings is maintained. In response to the applicant arguments, Figures 4A and 4B, steps 410 and 414 of Figure 4A, as well as steps 410, 414 and 416 of Figure 4B only show “Did transaction complete” “status bit remains set” and “reset status bit”; however, does not show the feature "retrying the first bus transaction and each subsequent non modifying bus transaction for the shared resource until the status bit is clear" as recited in claim 1.

Claims 3-6 recite ways to clear the status bit. Figures 4A and 4B, "CLEAR STATUS BIT" is shown in step 412 of Figures 4A, as well as steps 412 and 418 of Figure 4B, but claim 3, “clearing the status bit randomly;” claim 4, “clearing the status bit at periodic intervals;” claim 5, “wherein the periodical intervals are longer than a length of time for a bus transaction to complete;” claim 6, “ clearing the status bit using a pseudo-random method,” are not shown. The discussion for drawings with respect to claims 1 and 3-6 also apply to drawings with respect to claims 7-9.

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 10-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, “the wherein the status indicator is a status bit to indicate whether the second bus transaction completes, if the nonmodifying bus transactions complete, the status bit is cleared, otherwise status bit remains as being set, “ claim 10 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that

the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 11-21 contains the similar problems as claim 10

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 10-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 10, 15, and 17 recites the limitation "the second bus transaction" . There is insufficient antecedent basis for this limitation in the claim.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-2, 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert et al., U.S. Patent No. 6,041,376 (hereinafter Gilbert) in view of Arimilli et al., U.S. Patent No. 6,138,218 (hereinafter Arimilli).

As per claim 1, Gilbert shows a method of preventing live-lock in a multiprocessor system (e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

Identifying a first bus transaction that is a nonmodifying transaction on a shared resource (e.g. fig. 7, el. 76, col. 9, line 45-50);

identifying a second bus transaction that attempts to modify the shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that the second bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20);

checking whether the second bus transaction completes (e.g., fig. 8C, 120-122;, when the same requesting processor retried to get the requested data, the bus transaction is complete)

clearing the status flag if the second bus transaction completes (e.g., fig. 8C, 120-122; when the same requesting processor retried to get the requested data, the bus transaction is complete)

maintaining the status flag as being set if the second bus transaction does not complete (e.g., fig. 8C, 120-122; when it 's not the same requesting processor retried to get the requested data, the bus transaction is not complete, a flag is remained set); and

retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claim 2 Gilbert teaches clearing the status flag when the reissued second bus transaction completes (e.g., fig. 8C, el. 122). As stated above, Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag),

minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claim 4, Gilbert shows the use of clearing the status flag at periodic intervals (e.g., fig. 8C, el. 124). As stated above, Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claim 5, Gilbert shows the use of clearing the status flag at periodic intervals (e.g., fig. 8C, el. 124) and the period intervals are longer than a length of time for a bus transaction to complete (any desired value; e.g., col. 11, lines 29-44). As stated above, Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining

the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

10. Claims 3 and 6-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert et al., U.S. Patent No. 6,041,376, (hereinafter Gilbert) in view of Arimilli et al., U.S. Patent No. 6,138,218 (hereinafter Arimilli), and further in view of Donley et al., U.S. Patent No. 5,761,446 (hereinafter Donley).

As per claim 7, Gilbert shows the use of a method of preventing live-lock in a multiprocessor system(e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

issuing a first bus transaction to read a cache line (e.g. fig. 7, el. 76, col. 7, lines 5-55 and col. 9, lines 48-52);

granting the cache line for the first bus transaction (e.g., col. 7, lines 5-55; col. 8, lines 5-10; fig. 8C, els. 118, 116, or 122)

issuing a second bus transaction that attempts to modify the cache line (fig. 6, el. 50; fig. 7, el. 76; and col. 7, lines 5-55 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the cache line (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus

transaction which is after to access a cache line; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that the second bus transaction attempting to modify the cache line is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20);

checking whether the second bus transaction completes (e.g., fig. 8C, 120-122;, when the same requesting processor retried to get the requested data, the bus transaction is complete);

clearing the status flag if the second bus transaction completes (e.g., fig. 8C, 120-122; when the same requesting processor retried to get the requested data, the bus transaction is complete)

maintaining the status flag as being set if the second bus transaction does not complete (e.g., fig. 8C, 120-122; when it 's not the same requesting processor retried to get the requested data, the bus transaction is not complete, a flag is remained set)

resetting the status flag either as being set or as cleared (e.g., fig. 8C, 120-122; 124);

retrying the first bus transaction if the status flag is set (i.e., read request for the same cache line again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5);

reissuing the second bus transaction that attempts to modify the cache line (e.g., fig. 8C, el. 120 and col. 11, lines 20);

granting the cache line for the reissued second bus transaction if the status flag is set for the cache line (e.g., fig. 8C, el. 122 and col. 11, lines 9-21).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3. Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo-random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

As per claim 10, Gilbert shows the use of a multiprocessor computer system comprising:

a plurality of processors (e.g., figs. 1-2, els. 12, 14, 24);

a resource shared by the plurality of processors (e.g., figs .2-3, el. 26, 44, 36, 34);

at least one system bus interconnecting the shared resource and the plurality of processors (e.g., figs.1-2, el. 20, 22);

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on the at least one system bus by one of the processors (e.g. figures 3,7, el. 44, 70; and col. 9, lines 20-65); and

a status indicator associated with each of the plurality of buffers (e.g. figures 3,7, el. 44, 70; and col. 9, lines 20-65), and the status indicator being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the shared resource (e.g. fig. 7, el. 76, col. 7, lines 5-55 and col. 9, lines 48-52; i.e., read request for the same cache line again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5), wherein the modifying bus transaction has priority over the nonmodifying bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a cache line; e.g., col. 2, lines 43-50; col. 3, lines 1-8),

wherein the status indicator is a status flag to indicate whether the second bus transaction completes (e.g., fig. 8C, 120,122), if the nonmodifying bus transactions complete, the status flag is cleared (e.g., fig. 8C, 120,122) , otherwise status flag remains as being set (e.g., fig. 8C, 120,122), and the status bit is reset (e.g., fig. 8C, 122, 124).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3,

element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3. Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo-random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

As per claim 15, Gilbert shows the use of a multiple bus, multiprocessor computer system ((e.g., figs. 1-2, els. 12, 14, 24)comprising:

a plurality of processors (e.g., figs. 1-2, els. 12, 14, 24);

a plurality of data cache memories (e.g., fig. 3, el. 44);

a system memory shared by the plurality of processors (e.g., figs. 2, el. 26);

at least two buses interconnecting the system memory with the plurality of data cache memories and the plurality of processors (e.g., figs.1-2, el. 20, 22); and

a controller (e.g. figs. 2-3, el. 30) comprising:

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on one of the buses by one of the processors (e.g. figures 3,7, el. 44, 70; and col. 9, lines 20-65); and

a status indicator associated with each of the plurality of buffers (e.g. figures 3,7, el. 44, 70; and col. 9, lines 20-65), and the status indicator being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the system memory (e.g. fig. 7, el. 76, col. 7, lines 5-55 and col. 9, lines 48-52; i.e., read request for the same memory address again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5 wherein the modifying bus transaction has priority over the nonmodifying bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a cache line; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

wherein the status indicator is a status flag to indicate whether the second bus transaction completes (e.g., fig. 8C, 120,122), if the nonmodifying bus transactions complete, the status flag is cleared (e.g., fig. 8C, 120,122) , otherwise status flag remains as being set (e.g., fig. 8C, 120,122), and the status bit is reset (e.g., fig. 8C, 122, 124).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the

teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3. Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo-random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

As per claim 17, Gilbert shows the use of an integrated circuit comprising:

a bus interface to control a plurality of bus transactions (e.g. fig. 3, el. 42, 40);

a coherency module to maintain cache coherency for a plurality of cache lines (e.g., fig. 3, 36, 34); and

a buffer manager (e.g., fig. 3, 30, 32, 44) comprising,

a plurality of buffers (e.g. fig. 5A, els. 500), each one of the buffers to store information associated with one of the plurality of bus transactions received by the bus interface (e.g. figures 3,7, el. 44, 70; and col. 9, lines 20-65); and

a plurality of status indicators (e.g. figures 3,7, el. 44, 70, 36, 34; and col. 9, lines 20-65) being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the one of the cache lines at least

one of the status indicators associated with each one of the buffers (e.g. fig. 7, el. 76, col. 7, lines 5-55 and col. 9, lines 48-52; i.e., read request for the same cache line again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5), wherein the modifying bus transaction has priority over the nonmodifying bus transaction to access the cache lines (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a cache line; e.g., col. 2, lines 43-50; col. 3, lines 1-8),

wherein the status indicator is a status flag to indicate whether the second bus transaction completes (e.g., fig. 8C, 120,122), if the nonmodifying bus transactions complete, the status flag is cleared (e.g., fig. 8C, 120,122) , otherwise status flag remains as being set (e.g., fig. 8C, 120,122), and the status bit is reset (e.g., fig. 8C, 122, 124).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3. Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo-

random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

As per claims 3, 6, and 9, Gilbert shows the use of clearing the status flag by a counter where the counter can be any desired value (e.g., col. 11, lines 29-44). As stated above, Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3. Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo-random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

As per claim 8, Gilbert teaches clearing the status flag when the reissued second bus transaction completes (e.g., fig. 8C, el. 122). As stated above, Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

As per claims 11-14, 16,18-20, Gilbert shows the use of four processors are coupled to each one of the system buses (e.g., figs. 1-2, els. 12, 18, 24); the use of at least one system bus comprises two processor buses (e.g. figures 1-2, connections to nodes 1-4, to processors 24); four processors coupled to each one of the two processor buses (e.g. figures 1-2, els. 12, 18, 24; connections to nodes 1-4, to processors 24); an input/output bus (e.g. figure 2, connections to I/O); each one of the at least two buses is coupled to four of the processors (e.g. figures 1-2, els. 12, 18, 24; connections to nodes 1-4, to processors 24); the buffer manager further comprises logic to determine a type of bus transaction occurring on a bus (e.g. fig. 7, el. 76); the buffer manager further comprises logic to determine if two of the bus transactions are contending for a same

cache line (col. 11, lines 10-20); logic to reset all of the plurality of status indicators (e.g., fig. 8C, els. 124 or 122; col. 2, lines 51-60; and col. 11, lines 9-30, where all the status flag can be reset at different times).

11. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gilbert et al., U.S. Patent No. 6,041,376, (hereinafter Gilbert) in view of Arimilli et al., U.S. Patent No. 6,138,218 (hereinafter Arimilli), further in view of Donley et al., U.S. Patent No. 5,761,446 (hereinafter Donley), and further in view of Vogt et al., U.S. Patent No. 5,897,656, (hereinafter Vogt).

As per claim 21, the combination of Gilbert, Arimilli, and Donley does not show 64 buffers and 64 status indicators; however, Vogt shows the use of 64 buffers and 64 status indicators (e.g. figure 5A, els 500 and 502, 505 and col. 26, lines 15-20). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Vogt into the combine system of Gilbert, Arimilli, and Donley because it would allow a low latency and high bandwidth system.

12. Applicant's arguments filed 3/10/08 have been fully considered but they are not persuasive.

13. In the remarks, the applicant argued that neither Gilbert nor Arimilli teaches the features “checking whether the second bus transaction completes; clearing the status bit if the second bus transaction completes; maintaining the status bit as being set if the

second bus transaction does not complete; randomly resetting the status bit either as being set or as cleared" as recited in claim 1.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., randomly resetting the status bit either as being set or as cleared) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case, the combination of Gilbert and Arimilli teaches what in the claim are: Gilbert shows a method of preventing live-lock in a multiprocessor system (e.g. figs. 1-2 and 6-8C, col. 2, lines 7-50), the method comprising:

Identifying a first bus transaction that is a nonmodifying transaction on a shared resource (e.g. fig. 7, el. 76, col. 9, line 45-50);

identifying a second bus transaction that attempts to modify the shared resource (e.g. fig. 7, el. 76, col. 7, line 5 and col. 9, lines 48-52), wherein the second bus transaction has priority over the first bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a shared resource; e.g., col. 2, lines 43-50; col. 3, lines 1-8);

setting a status flag to indicate that the second bus transaction attempting to modify the shared resource is pending (e.g., fig. 8C, el. 110; and col. 9, line 63-65 and col. 11, lines 9-20);

checking whether the second bus transaction completes (e.g., fig. 8C, 120-122;, when the same requesting processor retried to get the requested data, the bus transaction is complete)

clearing the status flag if the second bus transaction completes (e.g., fig. 8C, 120-122; when the same requesting processor retried to get the requested data, the bus transaction is complete)

maintaining the status flag as being set if the second bus transaction does not complete (e.g., fig. 8C, 120-122; when it 's not the same requesting processor retried to get the requested data, the bus transaction is not complete, a flag is remained set); and

retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared (e.g. fig. 8C, els. 114-118 and 122; and col. 11, lines 9-20 and col. 9, lines 14-18).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3.

14. In the remarks, the applicant argued that neither Gilbert nor Arimilli teaches the features “checking whether the second bus transaction completes; clearing the status bit if the second bus transaction completes; maintaining the status bit as being set if the second bus transaction does not complete; randomly resetting the status bit either as being set or as cleared" as recited in claim 7.

The examiner disagreed with the applicant arguments. The combination of Gilbert, Arimilli, and Donley teaches the features as recited in claim 7. In particular, Gilbert teaches checking whether the second bus transaction completes (e.g., fig. 8C, 120-122;, when the same requesting processor retried to get the requested data, the bus transaction is complete);

clearing the status flag if the second bus transaction completes (e.g., fig. 8C, 120-122; when the same requesting processor retried to get the requested data, the bus transaction is complete)

maintaining the status flag as being set if the second bus transaction does not complete (e.g., fig. 8C, 120-122; when it 's not the same requesting processor retried to get the requested data, the bus transaction is not complete, a flag is remained set)

resetting the status flag either as being set or as cleared (e.g., fig. 8C, 120-122; 124);

retrying the first bus transaction if the status flag is set (i.e., read request for the same cache line again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5);

reissuing the second bus transaction that attempts to modify the cache line (e.g., fig. 8C, el. 120 and col. 11, lines 20);

granting the cache line for the reissued second bus transaction if the status flag is set for the cache line (e.g., fig. 8C, el. 122 and col. 11, lines 9-21).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e., two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3. Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo-random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63.

15. In the remarks, the applicant argued that neither Gilbert nor Vogt teaches the features “checking whether the second bus transaction completes; clearing the status

bit if the second bus transaction completes; maintaining the status bit as being set if the second bus transaction does not complete; randomly resetting the status bit either as being set or as cleared" with respect to claims 10, 15, and 17.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "checking whether the second bus transaction completes; clearing the status bit if the second bus transaction completes; maintaining the status bit as being set if the second bus transaction does not complete; randomly resetting the status bit either as being set or as cleared") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case, the combination of Gilbert and Arimilli teaches, for example what in the claim 10 are: Gilbert shows the use of a multiprocessor computer system comprising:

a plurality of processors (e.g., figs. 1-2, els. 12, 14, 24);

a resource shared by the plurality of processors (e.g., figs .2-3, el. 26, 44, 36, 34);

at least one system bus interconnecting the shared resource and the plurality of processors (e.g., figs.1-2, el. 20, 22);

a plurality of buffers, each one of the plurality of buffers associated with a bus transaction initiated on the at least one system bus by one of the processors (e.g. figures 3,7, el. 44, 70; and col. 9, lines 20-65); and

a status indicator associated with each of the plurality of buffers (e.g. figures 3,7, el. 44, 70; and col. 9, lines 20-65), and the status indicator being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the shared resource (e.g. fig. 7, el. 76, col. 7, lines 5-55 and col. 9, lines 48-52; i.e., read request for the same cache line again when data being modify or invalid; e.g. fig. 8C, els. 114-116; col. col. 6, line 55 and et seq.; col. 4, line 40 to col. 5), wherein the modifying bus transaction has priority over the nonmodifying bus transaction to access the shared resource (e.g., when a modify bus transaction is a first in time, it has priority over a nonmodifying bus transaction which is after to access a cache line; e.g., col. 2, lines 43-50; col. 3, lines 1-8),

wherein the status indicator is a status flag to indicate whether the second bus transaction completes (e.g., fig. 8C, 120,122), if the nonmodifying bus transactions complete, the status flag is cleared (e.g., fig. 8C, 120,122) , otherwise status flag remains as being set (e.g., fig. 8C, 120,122), and the status bit is reset (e.g., fig. 8C, 122, 124).

Gilbert does not specifically show the use of the status flag as a single bit. Arimilli shows the use of a flag as a single bit (e.g. col. 3, lines 8-12; and figure 3, element 318 and col. 8, lines 36-44). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Arimilli to the teaching of Gilbert because it would provide for the storage of the flag (i.e., maintaining the integrity of the flag), minimizing the storage requirements of the system by using a single bit, especially when the flag is used to show the use of one state or the other (i.e.,

two states) and allow other traffic to proceed and alleviate the prospect of a live-lock as taught by Arimilli, col. 3, lines 1-3. Gilbert and Arimilli do not specifically show the use of randomly or pseudo-randomly. Donley shows generating random number or Pseudo-random number (e.g., col. 3, lines 46-60). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to apply the teaching of Donley to the combine system of Gilbert and Arimilli because it would provide a random delay time, thereby optimizing live-lock avoidance and system performance as taught by Donley, col. 2, lines 61-63. Claims 15 and 17 have similar features to the features of claim 10.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and an alternate Friday from 8:45 a.m. to 5:15 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sough Hyung, can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Denise Tran/

Primary Examiner, Art Unit 2188